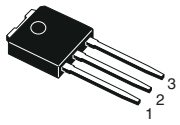
STD2NC45-1
STQ1NC45R-AP

N-channel 450V - 4.1Ω - 1.5A - IPAK - TO-92
SuperMESH™ Power MOSFET

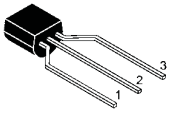
General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STD2NC45-1	450V	<4.5Ω	1.5A	30W
STQ1NC45R-AP	450V	<4.5Ω	0.5A	3.1W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- New high voltage benchmark



IPAK

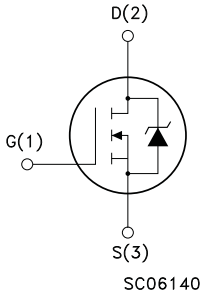


TO-92 (ammopak)

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application
  - Switch mode low power supplies (SMPS)
  - Low power, low cost CFL (compact fluorescent lamps)
  - Low power battery chargers

Order codes

Part number	Marking	Package	Packaging
STD2NC45-1	D2NC45	IPAK	Tube
STQ1NC45R-AP	Q1NC45R	TO-92	Ammopak

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2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 9

4 Package mechanical data 10

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		IPAK	TO-92	
V_{DS}	Drain-source voltage (V_{GS} = 0)	450		V
V_{GS}	Gate- source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25°C	1.5	0.5	A
I_D	Drain current (continuous) at T_C = 100°C	0.95	0.315	A
I_{DM} (1)	Drain current (pulsed)	6	2	A
P_{TOT}	Total dissipation at T_C = 25°C	30	3.1	W
	Derating factor	0.24	0.025	W/°C
dv/dt (2)	Peak diode recovery voltage slope	3		V/ns
T_{stg}	Storage temperature	–65 to 150		°C
T_j	Max. operating junction temperature			°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 0.5A$, di/dt ≤ 100 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		IPAK	TO-92	
Rthj-case	Thermal resistance junction-case max	4.1	--	°C/W
Rthj-amb	Thermal resistance junction-ambient max	100	120	°C/W
Rthj-lead	Thermal resistance junction-lead max	--	40	°C/W
T_l	Maximum lead temperature for soldering purpose	275	260	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	1.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AS}, V_{DD}=50V)	25	mJ

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} = 0	450			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C				1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.3	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 0.5A		4.1	4.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 0.5A		1.1		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		160 27.5 4.7		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 360V, I_D = 1.5A, V_{GS} = 10V, R_G = 4.7Ω *(see Figure 18)*		7 1.3 3.2	10	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

Table 6. Switching times

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 225V, I_D = 0.5A R_G = 4.7Ω V_{GS} = 10V *(see Figure 17)*		6.7 4		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 360V, I_D = 1.5A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 17)*		8.5 12 18		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				1.5 6.0	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.5A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1.5A, di/dt = 100A/µs V_{DD} = 100V, T_j = 150°C *(see Figure 22)*		225 530 4.7		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for IPAK

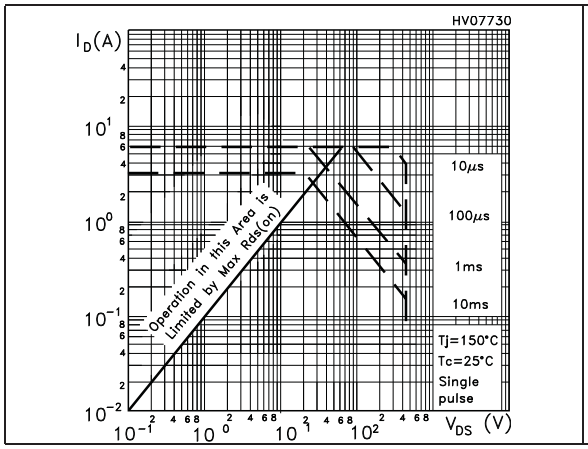


Figure 2. Thermal impedance for IPAK

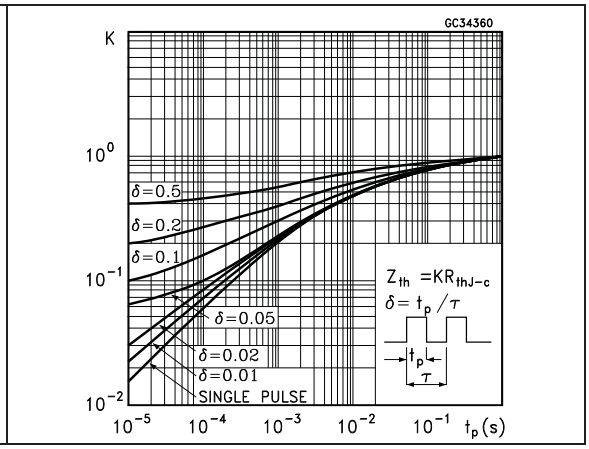


Figure 3. Safe operating area for TO-92

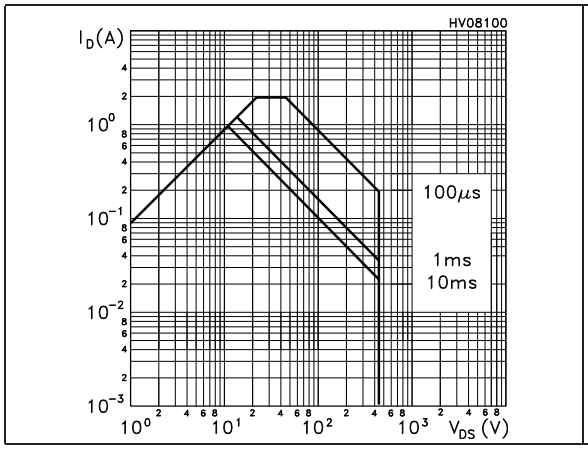


Figure 4. Thermal impedance for TO-92

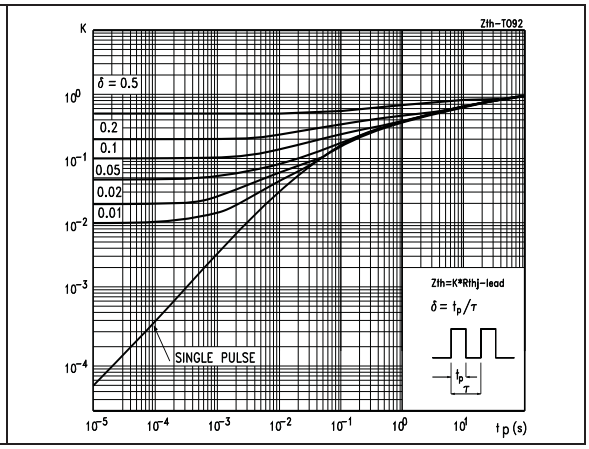


Figure 5. Output characterisics

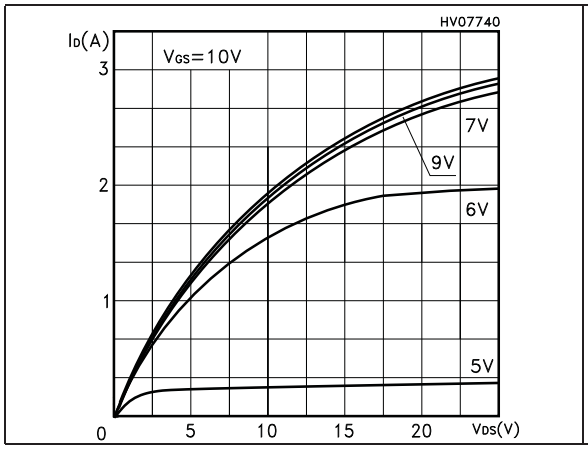


Figure 6. Transfer characteristics

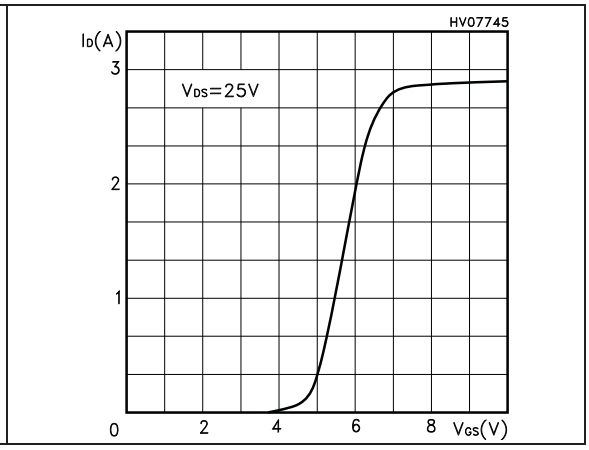


Figure 7. Transconductance

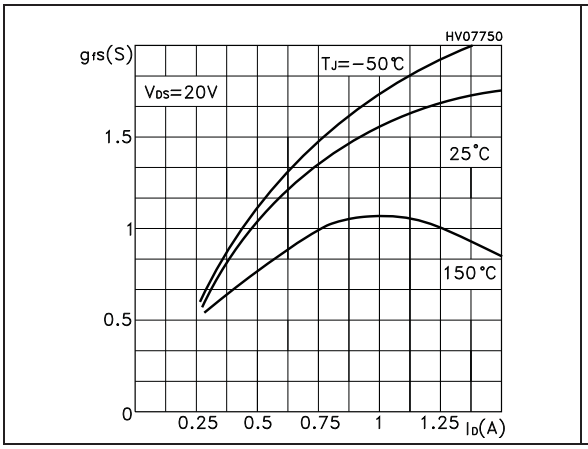


Figure 8. Static drain-source on resistance

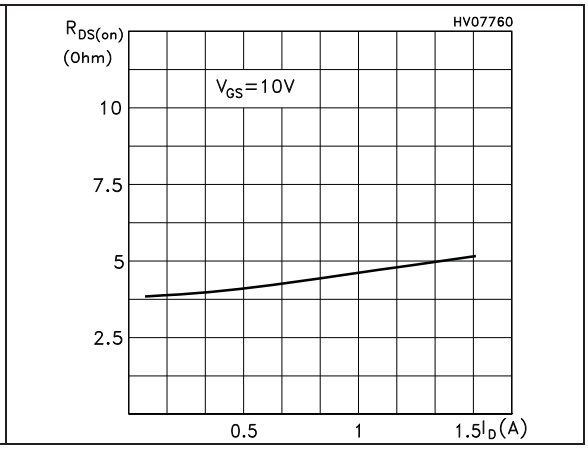


Figure 9. Gate charge vs gate-source voltage

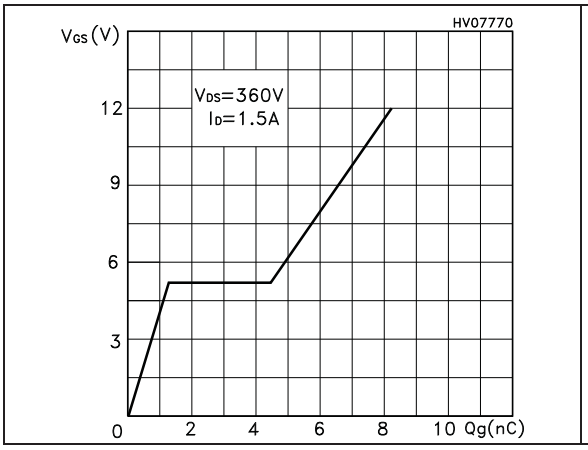


Figure 10. Capacitance variations

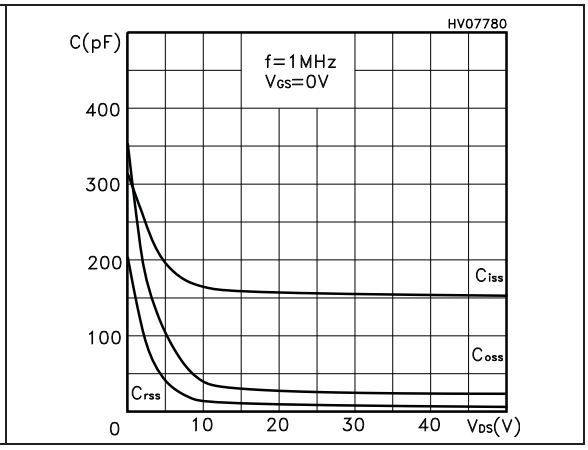


Figure 11. Normalized gate threshold voltage vs temperature

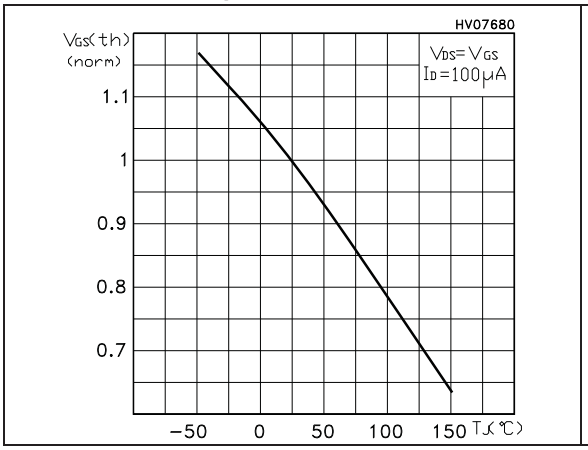


Figure 12. Normalized on resistance vs temperature

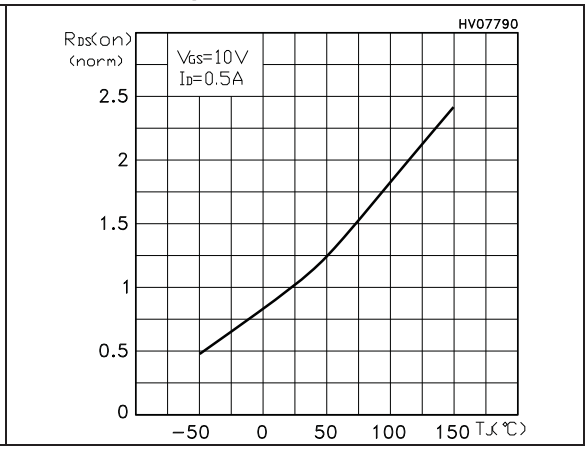


Figure 13. Source-drain diode forward characteristics

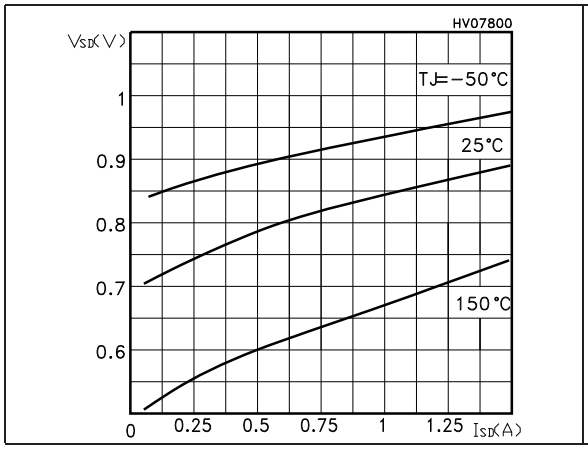


Figure 14. Normalized B_{VDSS} vs temperature

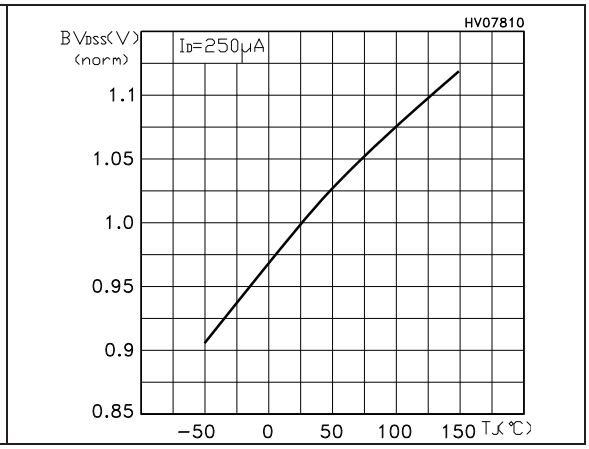


Figure 15. Max Id current vs Temperature

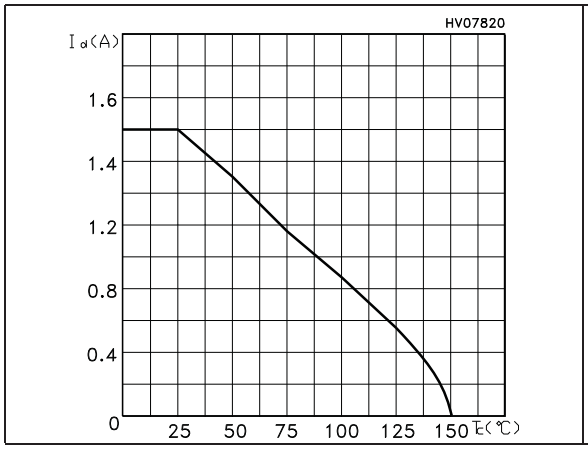
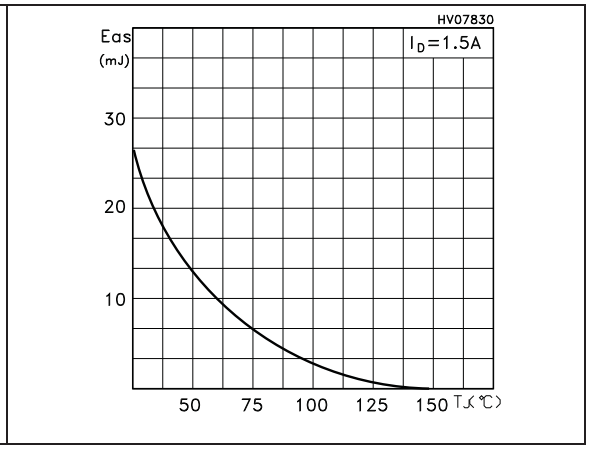


Figure 16. Maximum avalanche energy vs temperature



3 Test circuit

Figure 17. Switching times test circuit for resistive load

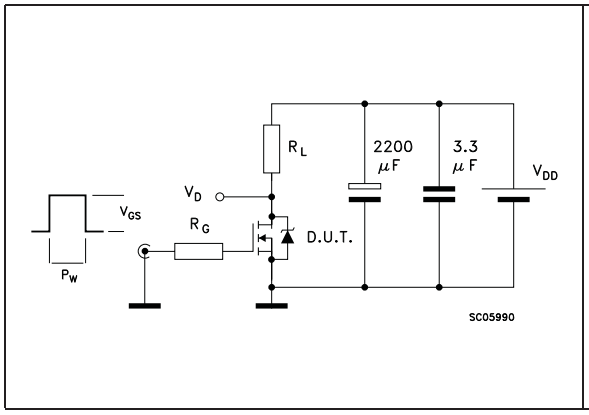


Figure 18. Gate charge test circuit

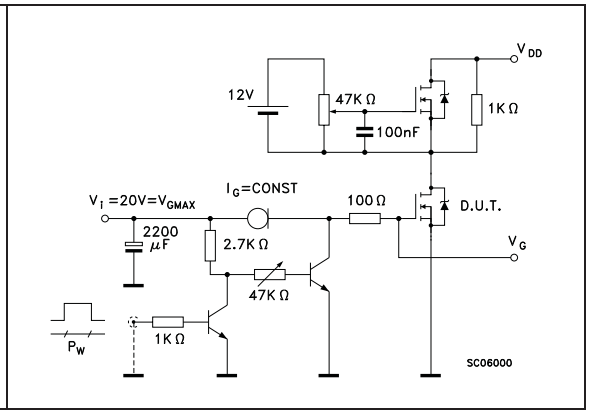


Figure 19. Test circuit for inductive load switching and diode recovery times

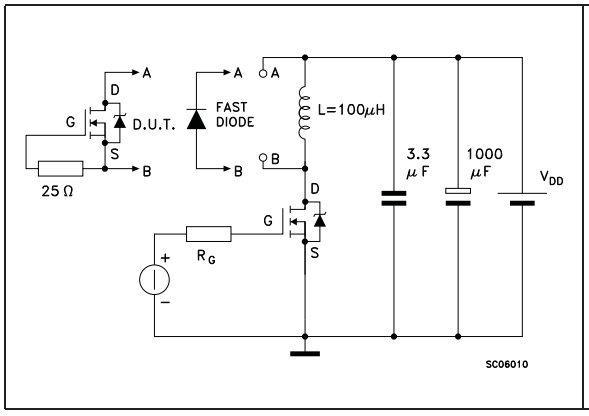


Figure 20. Unclamped Inductive load test circuit

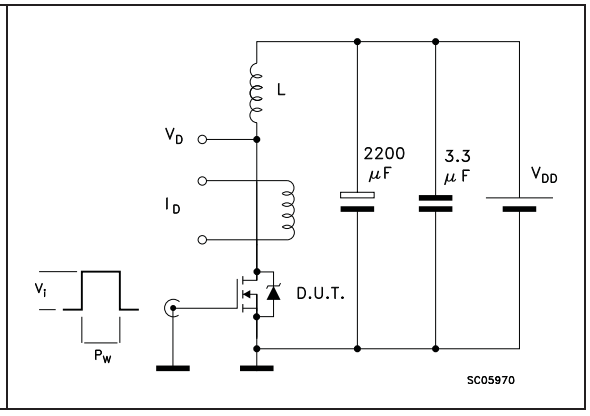


Figure 21. Unclamped inductive waveform

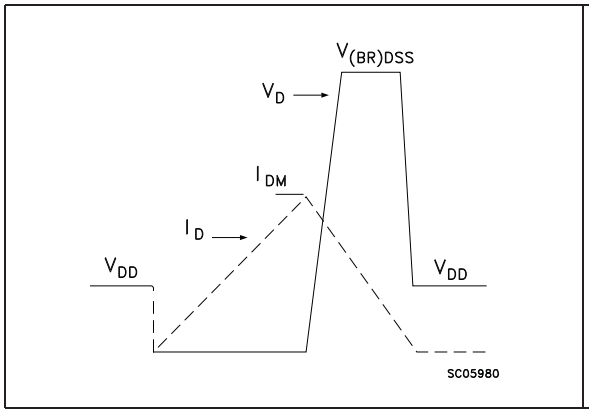
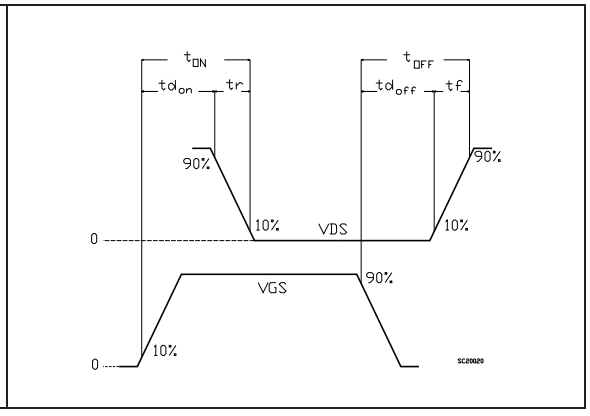


Figure 22. Switching time waveform

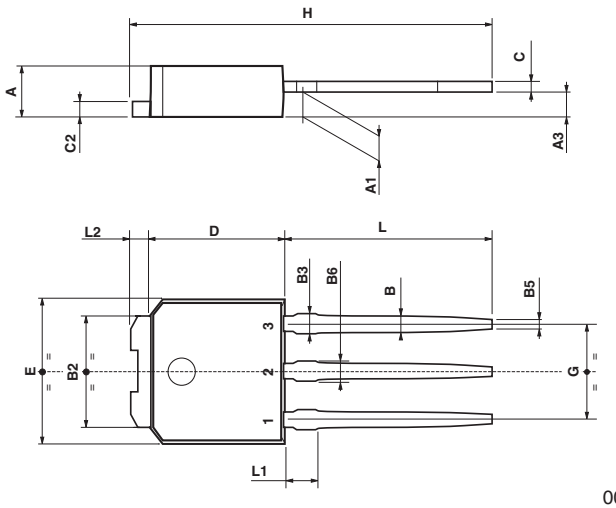


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-251 (IPAK) MECHANICAL DATA

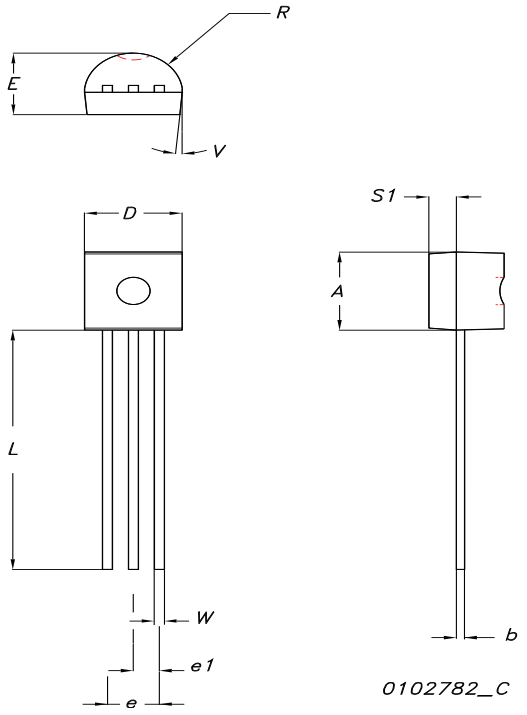
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

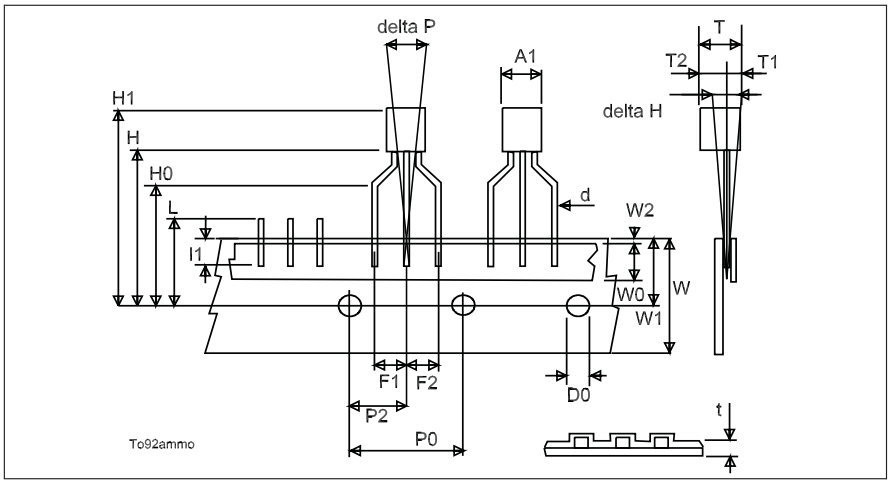
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	2	Complete version
12-Jul-2006	3	New template

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